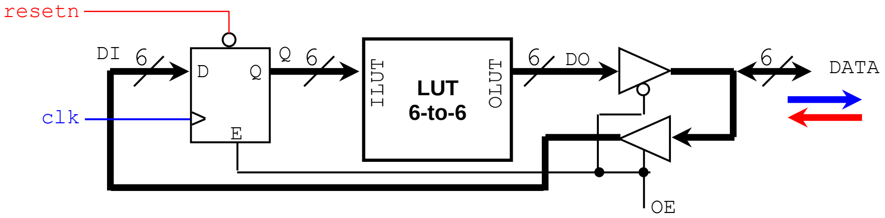
Final Exam

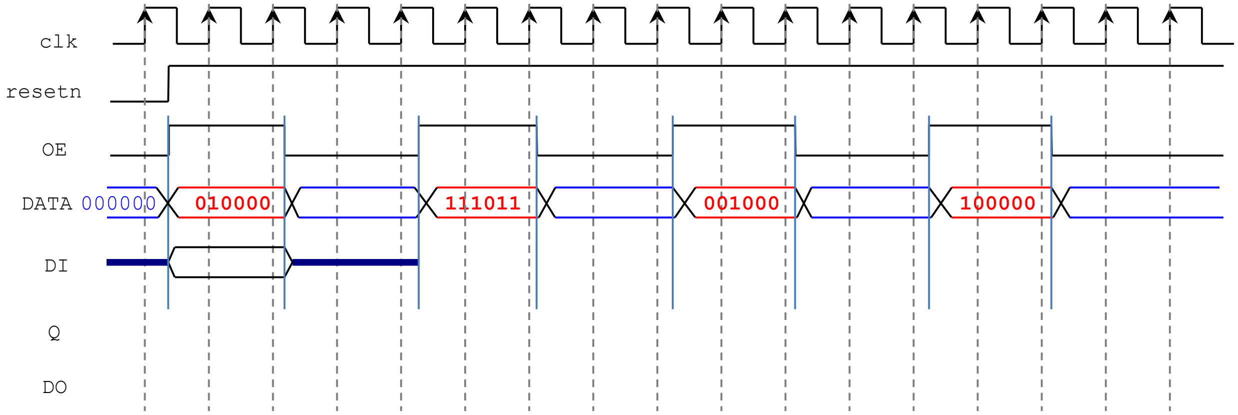
(December 8th @ 7:00 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (12 PTS)

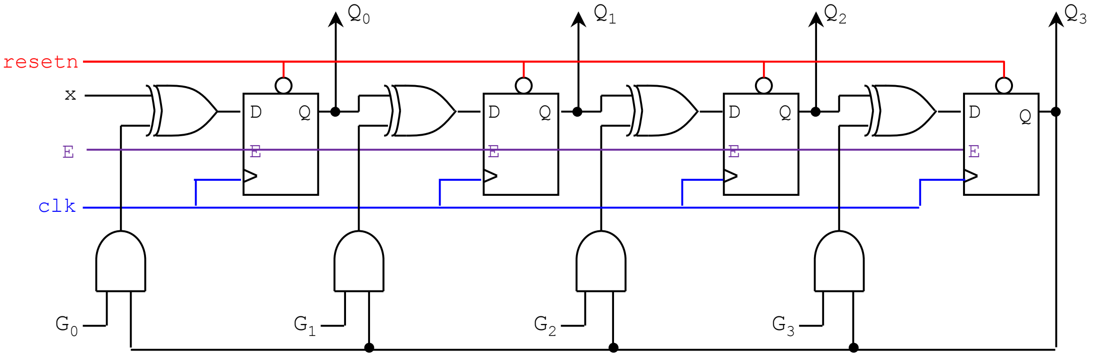
- Given the following circuit, complete the timing diagram.
  The LUT 6-to-6 implements the following function: $OLUT = \lfloor sqrt(ILUT) \rfloor$, where $ILUT$ is a 6-bit unsigned number.
  For example $ILUT = 35\ (100011_2) \rightarrow OLUT = \lfloor sqrt(35) \rfloor = 6\ (000110_2)$

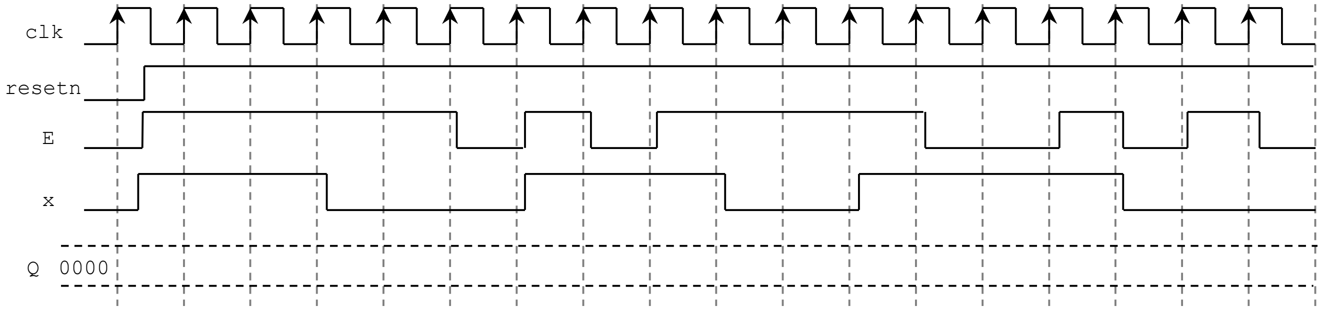




PROBLEM 2 (12 PTS)

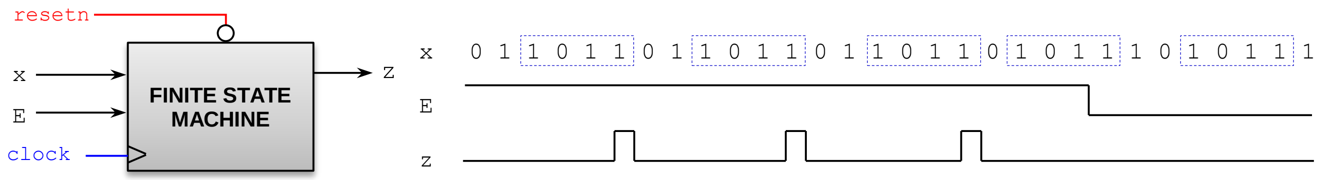
- Complete the timing diagram of the following circuit. $G = G_3G_1G_2G_0 = 1001$, $Q = Q_3Q_2Q_1Q_0$





PROBLEM 3 (22 PTS)

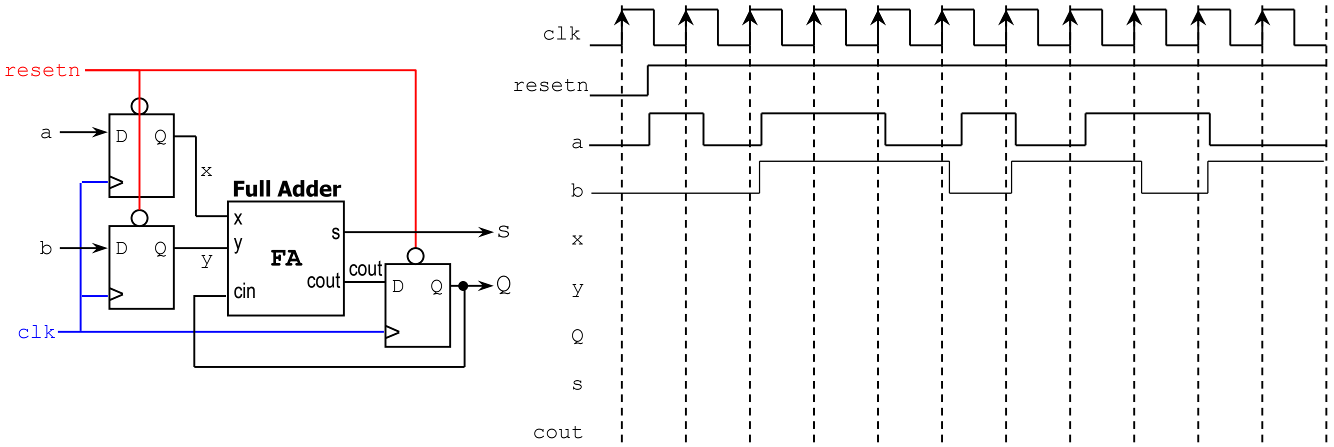
- Sequence detector: The machine has to generate $z = 1$ when it detects the sequence 1011. Once the sequence is detected, the circuit looks for a new sequence.
- The signal E is an input enable: It validates the input x, i.e., if $E = 1$, x is valid, otherwise x is not valid.


resetn
x
E
clock
FINITE STATE MACHINE
z
x 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 0 1 1 1 0 1 0 1 1 1
E
z

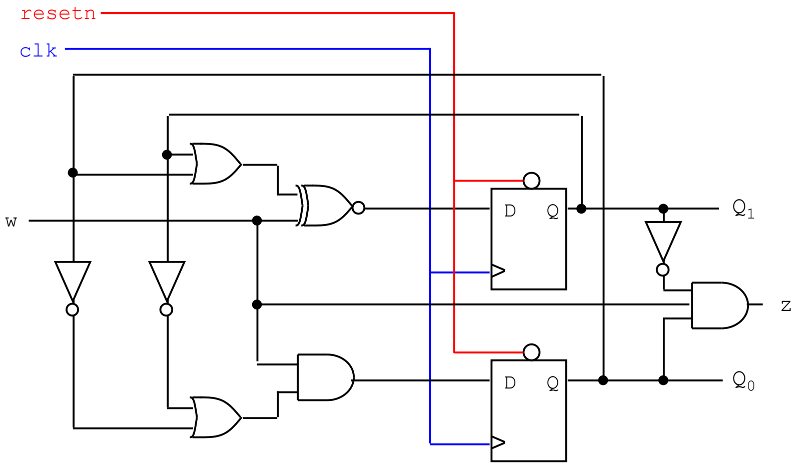
- Draw the State Diagram (any representation), State Table, and the Excitation Table of this circuit with inputs E and x and output z. Is this a Mealy or a Moore machine? Why? (15 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (4 pts)
- Sketch the circuit. (3 pts)

PROBLEM 4 (20 PTS)

- Complete the timing diagram of the circuit shown below: (8 pts)



- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following Finite State Machine: (12 pts)

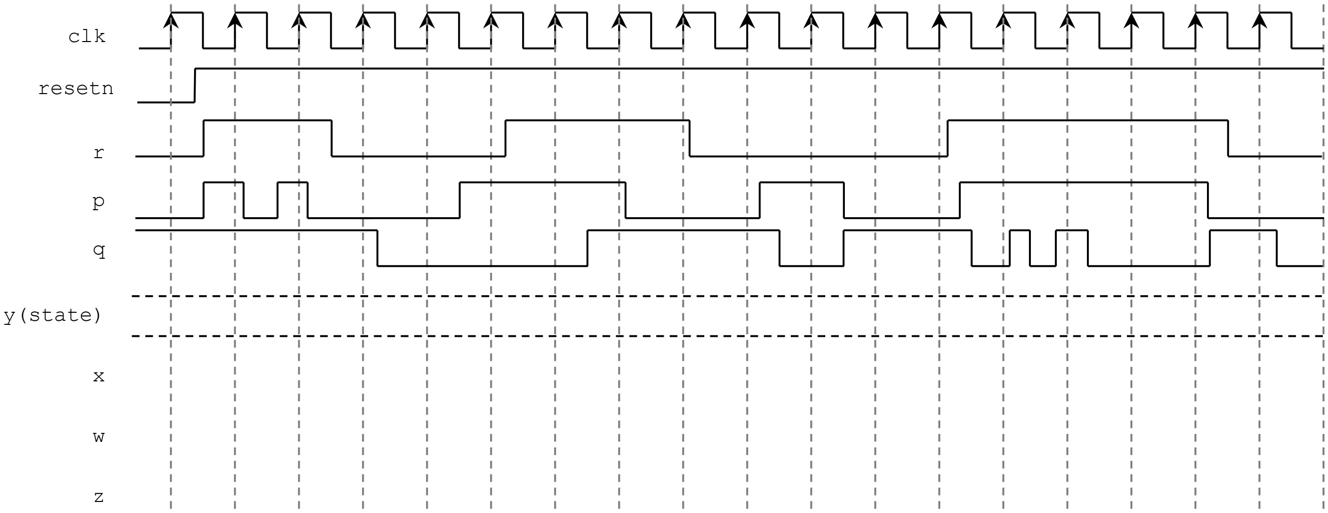


PROBLEM 5 (16 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

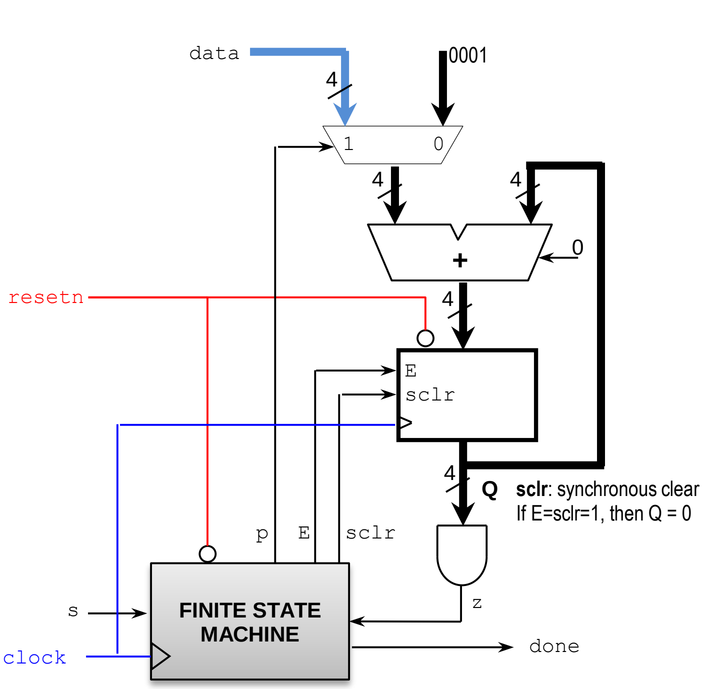
```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, resetn: in std_logic;
          r, p, q: in std_logic;
          x, w, z: out std_logic);
end circ;
```

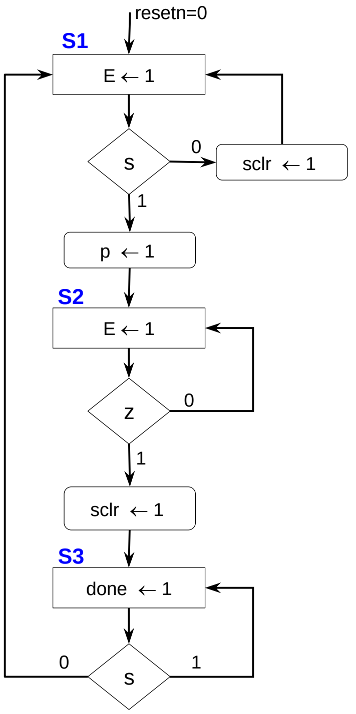
```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, r, p, q)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if r = '1' then
               y <= S2;
            else
               if p = '1' then y <= S3; else y <= S1; end if;
            end if;

          when S2 =>
            if p = '1' then y <= S1; else y <= S3; end if;

          when S3 =>
            if q = '1' then y <= S3; else y <= S2; end if;

        end case;
     end if;
  end process;

  Outputs: process (y, r, p, q)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if r = '0' then
                       if p = '0' then
                          w <= '1'; x <= '1';
                       end if;
                    end if;

         when S2 => if q = '0' then x <= '1'; end if;
                    if p = '0' then z <= '1'; end if;

         when S3 => if q = '0' then x <= '1'; end if;
      end case;
  end process;
end behavioral;
```

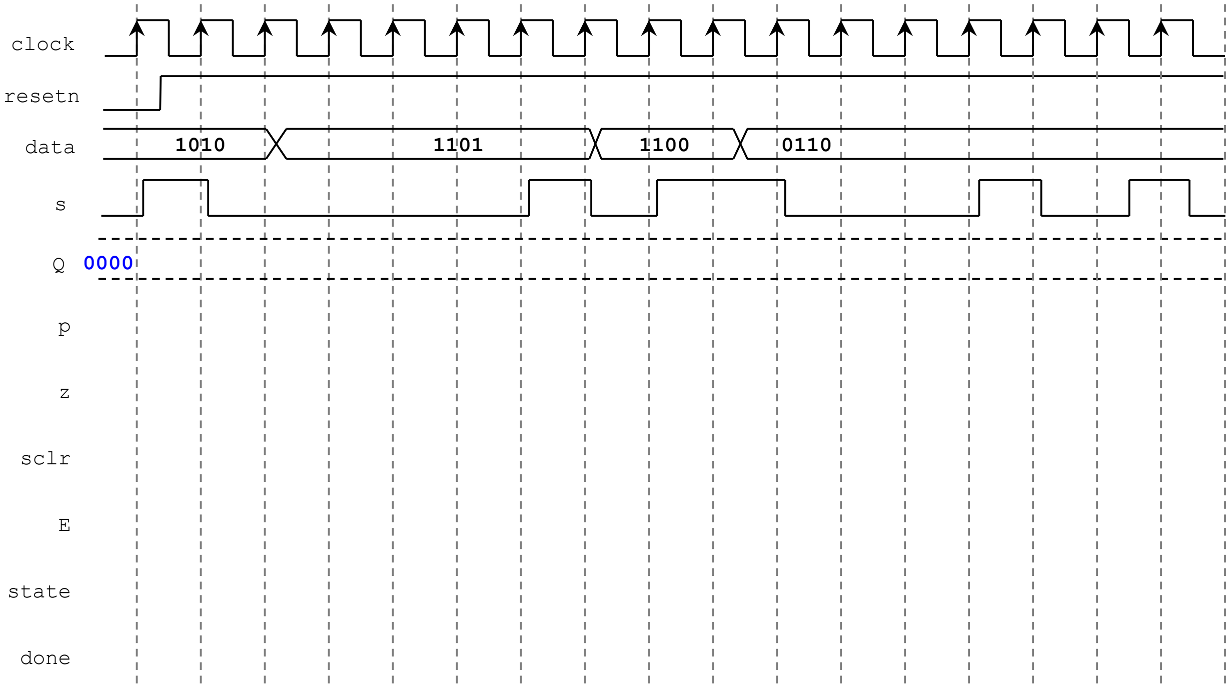


PROBLEM 6 (18 PTS)

- Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a datapath circuit.


data
4
0001
1
0
4
4
+
0
resetn
4
E
sclr
4
Q
sclr: synchronous clear
If E=sclr=1, then Q = 0
p
E
sclr
z
s
FINITE STATE MACHINE
clock
done


resetn=0
S1
E ← 1
s
0
sclr ← 1
1
p ← 1
S2
E ← 1
z
0
1
sclr ← 1
S3
done ← 1
0
s
1


clock
resetn
data
s
Q
p
z
sclr
E
state
done